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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/827,360	04/20/2004	Richard Carl Phelps	0120-030	2608

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EXAMINER	
CLEARY, THOMAS J	
ART UNIT	**PAPER NUMBER**
2111	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/30/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/827,360	PHELPS ET AL.	
	Examiner	Art Unit	
	Thomas J. Cleary	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 November 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the Applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the Applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 4-6, 8, and 12 are rejected under 35 U.S.C. 102(e) as being anticipated by US Patent Number 6,064,679 to Hashemi et al. ("Hashemi").

3. In reference to Claim 1, Hashemi discloses an apparatus for use in a computer system comprising: a pipeline bus architecture, in which data traverses the bus architecture over a plurality of system clock cycles (See Column 6 Lines 6-15); a plurality of modules adapted for selective connection to the bus architecture (See Figure 1A Numbers 126, 128, 130, and 132); wherein the bus architecture comprises: a plurality of bus connection units (See Figure 3 Number 300); and a plurality of bus portions arranged in series, each bus portion, except the last in the series, being connected to the next portion in the series by way of a bus connection unit (See Figure

1A Numbers 114, 116, 118, 120, and 122), each of the bus connection units including multiplexer circuitry for selectively connecting a module to the bus architecture (See Figure 3 Number 304), wherein the modules are connected to the bus architecture only by way of the bus connection units and in response to operation of the multiplexer circuitry (See Figure 3 Number 300 and Column 8 Lines 30-52).

4. In reference to Claim 4, Hashemi discloses the limitations as applied to Claim 1 above. Hashemi further discloses a primary pipelined bus (See Figure 1A Number 114) and secondary pipelined bus (See Figure 1A Numbers 116, 118, and 120) interconnected by an interface (See Figure 1A Number 104), a first plurality of modules connected to the primary bus (See Figure 1A Number 126), and a second plurality of modules connected to the secondary bus (See Figure 1A Numbers 128 and 130) by means of respective said bus connection units (See Figure 3 Number 300).

5. In reference to Claim 5, Hashemi discloses the limitations as applied to Claim 1 above. Hashemi further discloses that a central arbitration unit arbitrates between the modules in order to grant access to the bus architecture (See Column 1 Lines 43-45).

6. In reference to Claim 6, Hashemi discloses the limitations as applied to Claim 5 above. Hashemi further discloses a primary pipelined bus (See Figure 1A Number 114) and secondary pipelined bus (See Figure 1A Numbers 116, 118, and 120) interconnected by an interface (See Figure 1A Number 104), a first plurality of modules

connected to the primary bus (See Figure 1A Number 126), and a second plurality of modules connected to the secondary bus (See Figure 1A Numbers 128 and 130) by means of respective said bus connection units (See Figure 3 Number 300).

7. In reference to Claim 8, Hashemi discloses the limitations as applied to Claim 4 above. Hashemi further discloses that the primary bus is one pipeline stage in length (See Figure 1A).

8. In reference to Claim 12, Hashemi discloses the limitations as applied to Claim 1 above. Hashemi further discloses a computer system comprising the apparatus of Claim 1 (See Figures 1A and 3).

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 2 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hashimi.

11. In reference to Claim 2, Hashimi discloses the limitations as applied to Claim 1 above. Hashimi does not explicitly disclose that each bus connection unit includes output circuitry connected to the bus portions to which the unit is connected, the output circuitry being tailored to optimize the signal characteristics for the length of the bus portions concerned. However, Official Notice is taken that the use of a bus driver having optimized signal characteristics for the bus segment it is connected to is well known in the art.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Hashimi using output circuitry having optimized signal characteristics for the bus, resulting in the invention of Claim 2, because optimizing the signal characteristics allows an increase in efficiency and reduction in power and cost, which are beneficial when constructing a device.

12. In reference to Claim 3, Hashimi discloses the limitations as applied to Claim 1 above. Hashimi does not explicitly disclose that the bus portions are all equal in physical length. The portion of the specification describing the length of the bus portions indicates that equal length bus portions are the preferred length with no further details (See Page 7 Lines 26-27).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Hashimi using bus portions that are equal in length, resulting in the invention of Claim 3, because Applicant has not disclosed that using equal length bus portions provides and advantage, is used for a particular

purpose, or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected Applicant's invention to perform equally well with either the bus lengths disclosed by Hashimi or the claimed equal length bus portions, because both perform the same function of providing a means of communications between components.

13. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hashimi as applied to Claim 4 above, and further in view of US Patent Number 6,057,863 to Olarig ("Olarig").

14. In reference to Claim 7, Hashimi discloses the limitations as applied to Claim 4 above. Hashimi does not disclose that the first plurality of modules are latency intolerant and the second plurality of modules are latency tolerant. Olarig teaches an FC-AL system, such as that of Hashimi, in which a plurality of latency intolerant modules are connected to one portion of a bus (See Figure 1 Numbers 102, 104, and 106) through a bus interface (See Figure 1 Number 150), and a plurality of latency tolerant modules are connected to another portion of the bus (See Figure 1 Numbers 158 and 160, Column 7 Lines 57-60 and Column 8 Lines 28-36).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Olarig using the improved FC-AL of Hashimi, resulting in the invention of Claim 7, in order to allow the loop to be maintained despite removal or failure of a node port (See Column 1 Lines 56-60 of Hashimi) and to

avoid clock jitter and thus increase the cascadability of the hubs (See Column 3 Lines 54-67 of Hashimi).

15. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hashimi as applied to Claim 1 above, and further in view of US Patent Number 5,128,926 to Perlman et al. ("Perlman").

16. In reference to Claim 9, Hashimi teaches the limitations as applied to Claim 1 above. Hashimi does not teach that transactions involving data in excess of a predetermined size are split into a plurality of data packets of fixed size, said packets being independently arbitrated. Perlman teaches splitting a large packet into pieces which are smaller than the maximum packet size and transmitting the smaller packets separately (See Column 2 Lines 55-58).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Hashimi with the packet splitting of Perlman, resulting in the invention of Claim 9, in order to relieve the computation burden by reducing the probability of errors in transmission (See Column 2 Line 64 – Column 3 Line 14 of Perlman).

17. Claims 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hashimi as applied to Claim 1 above, and further in view of US Patent Number 5,925,118 to Revilla et al. ("Revilla").

18. In reference to Claim 10 Hashimi teaches the limitations as applied to Claim 1 above. Hashimi does not teach separate read, write, and transaction buses. Revilla teaches the use of separate read (See Figure 1 Number 34), write (See Figure 1 Number 32), and transaction buses (See Figure 1 Number 36).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Hashimi with the split bus system of Revilla, resulting in the invention of Claim 10, in order to provide a high throughput of data between functions (See Column 2 Lines 17-31 of Revilla).

19. In reference to Claim 11 Hashimi teaches the limitations as applied to Claim 1 above. Hashimi does not teach that the bus architecture has a width sufficient to permit read and write request transactions to alternate in successive system clock cycles. Revilla teaches the use of separate read (See Figure 1 Number 34), write (See Figure 1 Number 32), and transaction buses (See Figure 1 Number 36) which have a width sufficient to permit read and write request transactions to alternate in successive system clock cycles (See Column 3 Lines 12-26).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Hashimi with the split bus system of Revilla, resulting in the invention of Claim 11, in order to provide a high throughput of data between functions (See Column 2 Lines 17-31 of Revilla).

20. Claims 1, 5, and 12 are rejected under 35 U.S.C. 102(e) as being anticipated by US Patent Number 6,055,228 to DeKoning et al. ("DeKoning") and US Patent Number 5,548,733 to Sarangdhar et al. ("Sarangdhar").

21. In reference to Claim 1, DeKoning discloses an apparatus for use in a computer system comprising: a bus architecture, in which data traverses the bus architecture over a plurality of system clock cycles (See Column 1 Lines 42-56); a plurality of modules adapted for selective connection to the bus architecture (See Figure 7A Number 702); wherein the bus architecture comprises: a plurality of bus connection units (See Figures 5 and 7 Numbers 516 and 518); and a plurality of bus portions arranged in series, each bus portion, except the last in the series, being connected to the next portion in the series by way of a bus connection unit (See Figures 5 and 7 Numbers 550-553), each of the bus connection units including multiplexer circuitry for selectively connecting a module to the bus architecture (See Figure 6 Number 600), wherein the modules are connected to the bus architecture only by way of the bus connection units and in response to operation of the multiplexer circuitry (See Figure 6 Number 600 and Column 11 Line 30 – Column 12 Line 9). DeKoning does not disclose that the bus is a pipelined bus. Sarangdhar teaches the use of a pipelined bus (See Column 1 Lines 20-28).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of DeKoning with the pipelined bus of

Sarangdhar, resulting in the invention of Claim 1, in order to allow multiple transactions to be processed concurrently (See Column 1 Lines 20-28 of Sarangdhar).

22. In reference to Claim 5, DeKoning and Sarangdhar disclose the limitations as applied to Claim 1 above. DeKoning further discloses that a central arbitration unit arbitrates between the modules in order to grant access to the bus architecture (See Column 1 Lines 57-67).

23. In reference to Claim 12, Hashemi discloses the limitations as applied to Claim 1 above. Hashemi further discloses a computer system comprising the apparatus of Claim 1 (See Figure 7).

Response to Arguments

24. Applicant's arguments with respect to Claims 1-12 have been considered but are moot in view of the new ground(s) of rejection.

25. Applicant has argued that certain features of the invention are discussed in the Specification at Page 29 Line 31 – Page 30 Line 9 (See Page 6 Paragraph 3). In

response, the Examiner notes that the feature does not appear in the identified section of the Specification, but instead appears to be at Page 30 Lines 17-28.

26. Applicant has argued that certain features of the invention are discussed in the Specification at Page 1 Lines 11-13 (See Page 6 Paragraph 4). In response, the Examiner notes that the feature does not appear in the identified section of the Specification, but instead appears to be at Page 1 Lines 17-19.

27. Applicant has argued that the bus connection unit that performs the connection enables a module to communicate with another via the bus and is the only means by which the module connects with the bus (Sere Page 7 Paragraph 1 and Page 9 Paragraph 2). Applicant has further argued and claimed that the modules are only connected, and can only be connected, to the bus through the bus connection units and the multiplexer circuitry within (See Page 9 Paragraph 3 – Page 10 Paragraph 1). It is unclear how a module can receive data from the bus (and thus receive data from another device), through the multiplexer with which it connects to the bus, as a multiplexer only allows data to flow through it in one direction.

28. Applicant has argued that the modules are more complex than registers (See Page 6 Paragraph 4). In response, the Examiner will interpret the modules as more complex than registers, as described in the Specification on Page 1 Lines 17-19.

29. Applicant has argued that the bus is purely for communication and contains no processing facility (See Page 9 Paragraph 2). In response, the Examiner will interpret the bus as such.

Conclusion

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Thomas J. Cleary whose telephone number is 571-272-3624. The Examiner can normally be reached on Monday-Thursday (7-3), Alt. Fridays (7-2).

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Mark Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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